REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 2, and 4 through 19 remain in this case. Claims 1, 2, 4, 5, 8 through 11, and 13 through 16 are amended. Claims 3 and 20 through 42 are canceled.

The specification is objected to because of the use of the word "irregardless". The specification is amended to correct this pet peeve of the Examiner.[1] No new matter is presented.

To advance the prosecution of this case, claims 20 through 42 are canceled, without prejudice to their being presented in a continuing or divisional application.

The cancellation of claim 42 obviates the objection to that claim.

All claims were rejected under §102(b) as anticipated by the Wells reference[2].

Regarding claims 1, 8, and 13, the Examiner asserted that the Wells reference teaches that it is normal in flash memory to map a plurality of logical blocks to a physical block and to provide the associated contents with those logical blocks to the physical block. Specific additional limitations in the claims dependent on these independent were also found by the Examiner in the Wells reference.

Claim 1 is amended to overcome the rejection, and also for clarity. Amended claim 1 now requires that each of the plurality of logical blocks include a plurality of logical pages arranged in groups. Amended claim 1 further requires that the at least one criterion used in the identifying step comprises its contents being associated with a number of groups of logical pages fewer than a first limit. The specification clearly supports this logical organization of the non-volatile memory and an example of the identifying of a logical block suitable for mapping to a

[1] This pet peeve is shared by the undersigned.

shared physical block,[3] and as such no new matter is presented by this amendment. Claim 1 is further amended for clarity.

Claims 2, 4, and 5 are similarly amended for clarity, and for consistency with the amendment to claim 1, upon which they depend. No new matter is presented by the amendment to these dependent claims. Claim 3 is canceled, considering the amendment to claim 1.

Applicants submit that amended claim 1 and its dependent claims are all novel over the Wells reference, on the grounds that the reference fails to disclose logical blocks that include a plurality of logical pages arranged in groups, and fails to disclose the identifying of a first logical block that has its contents associated with a number of groups of logical pages fewer than a first limit, as claimed.

The Wells reference does mention "logical blocks".[4] However, the reference defines its "logical block" as a pairing of physical "subblocks" in which odd bytes of data are stored on a subblock in one flash memory chip, and even bytes of data are stored on a subblock in another flash memory chip. To the extent this "logical block" differs from a physical block, it is by way of the splitting of odd and even bytes of data between subblocks in different integrated circuits. There is no other logical "block" arrangement of data disclosed by the Wells reference, nor is there any teaching in the Wells reference regarding the arrangement of this so-called logical block, or its internal structure. Accordingly, Applicants submit that the Wells reference nowhere disclose the requirement of amended claim 1 that each of the plurality of logical blocks includes a plurality of logical pages arranged in groups.

Applicants also submit that the Wells reference also falls short of amended claim 1 because it fails to disclose the identifying of a first logical block meeting a criterion that its contents are associated with a number of groups of logical pages fewer than a first limit. As mentioned above, the Wells reference wholly fails to disclose the internal arrangement of its

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[2] U.S. Patent No. 5,341,339, issued August 23, 1994 to Wells.
[3] *See, e.g.,* specification of S.N. 10/676,652, at page 11, lines 9 through 15.
[4] *See* Wells, *supra,* column 2, line 41 through column 3, line 2. Another use of the term "logical blocks" appears at column 11, lines 37, but without any additional context relative to that of the column 2 reference.

logical blocks, other than odd and even bytes being stored in subblocks of different integrated circuits; for this reason alone, Applicants submit that the Wells reference necessarily fails to disclose the identifying of the first logical block based on the criterion now recited in amended claim 1.

The Examiner asserted, relative to original claim 3, that the Wells reference teaches the identifying of a logical block based on its contents associated with less than a first number of groups in that block.[5] Applicants disagree with this interpretation of the reference. The cited portion of the Wells reference refers to the "cleaning up" of physical block as the result of a determination that more than a given percentage (*e.g.*,80%) of its capacity contains "dirty" (*i.e.*, obsolete) data.[6] The reference does not refer to a logical block in making this determination, nor does it determine whether the contents of any block (logical or otherwise) are associated with fewer than a number of groups of pages (logical or otherwise) fewer than a limit. The clean up process in the specifically cited portion of the reference simply describes the locating of a valid physical sector having sufficient space to receive valid data from the physical block being cleaned up.[7] Nowhere does the reference disclose any decision based upon the contents of a logical block, much less according to the criterion of amended claim 1, which is not surprising considering that the Wells reference nowhere refers to the internal arrangement of a logical block for any purpose.

For these reasons, Applicants submit that amended claim 1 and its dependent claims are novel over the Wells reference.

Applicants further submit that there is no suggestion from the prior art to modify the teachings of the Wells reference in such a manner as to reach amended claim 1. Such lack of suggestion is apparent from the operation of the flash memory of the Wells reference itself, in which sectors of data are simply written sequentially to sectors in physical blocks of the memory, without regard to any correlation between logical blocks (in the sense of amended claim 1, which

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[5] Office Action of November 28, 2005, page 3 (*citing* Wells, *supra,* at column 11, lines 20 through 32).
[6] Wells, *supra,* column 10, line 15 through column 11, line 19.
[7] Wells, *supra,* column 11, lines 20 through 32.

have logical pages) and physical blocks.[8] According to the Wells reference, logical sector numbers are listed in a lookup table against physical sector numbers for later retrieval.[9] No mapping of logical blocks to physical blocks, much less merging of more than one logical block to a single physical block, is disclosed or suggested by the reference. Nor do any of the other references of record provide any suggestion to modify the method of operation disclosed by the Wells reference in such a manner as to reach amended claim 1.

In addition, the invention of amended claim 1 provides important advantages over the prior art. For example, the ability to map more than one logical block to a single physical block, as enabled by the method of amended claim 1, extends the useful life of the flash memory, reduces the spreading of growing defects by increasing the size of a pool of available physical blocks.[10] These important advantages stem directly from the difference between amended claim 1 and the prior art, and as such support the patentability of amended claim 1 and its dependent claims.

For these reasons, Applicants respectfully submit that amended claim 1 and its dependent claims are not only novel but are patentably distinct over the prior art of record, including the Wells reference upon which the rejection is based.

Claim 8 is also amended to overcome the rejection. Amended claim 8 now requires that each logical block includes a plurality of logical pages arranged in groups, and that the at least one criterion is met by the contents of the first logical block being associated with a number of groups of logical pages fewer than a first limit. Applicants submit that the specification fully supports this amendment to claim 8,[11] and that therefore no new matter is presented by this amendment.

Claims 9 through 11 are amended for clarity, and for consistency with the amendment to claim 8, upon which they depend.

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[8] Wells, *supra,* column 6, line 18 through column 7, line 25.
[9] Wells, *supra,* column 6, lines 63 through 67.
[10] Specification, *supra,* page 12, line 27 through page 13, line 8.
[11] *See,* specification, *supra, e.g.,* at page 11, lines 9 through 15.

For similar reasons as discussed above relative to amended claim 1, Applicants submit that amended claims 8 through 11 and claim 12 are novel and patentably distinct over the prior art of record in this case, including the Wells reference.

Specifically, Applicants submit that amended claim 8 is novel over the Wells reference because the reference fails to disclose the recited arrangement of the first logical block, as having logical pages arranged in groups, and fails to disclose means for identifying a first logical block by that logical block having contents associated with a number of groups of logical pages fewer than a first limit. As discussed above, the Wells reference fails to disclose logical blocks whatsoever, except with respect to a logical block that is realized by odd and even bytes of data stored in subblocks of different integrated circuits. Not only does the Wells reference fail to disclose logical blocks in the context of claim 8, but the Wells reference completely fails to disclose or suggest any arrangement of such logical blocks beyond this odd/even physical storage; nowhere does the reference disclose a logical block that includes a plurality of logical pages arranged in groups as claimed. And because of this lack of disclosure, the Wells reference necessarily fails to disclose the identifying of a logical block according to the criterion specified by amended claim 8, relative to how many of its groups of logical pages are associated with its contents. Nor do the teachings of the Wells reference regarding the clean up of physical blocks having too high of a percentage of "dirty" data pertain to means for identifying of a first logical block as claimed, much less anticipate such means. Accordingly, Applicants submit that the Wells reference falls short of the requirements of amended claim 8, and that therefore claims 8 through 12 are novel over the reference.

Also as discussed above relative to claim 1, Applicants submit that there is no suggestion from the prior art to modify the teachings of the Wells reference in such a manner as to reach amended claim 8 and its dependent claims. The Wells reference itself provides no such suggestion, considering its sequential sector-based operation without regard to any other logical arrangement, much less as recited in amended claim 8. The other references of record also provide no suggestion in this regard. Furthermore, the important advantages that result from the very differences between amended claim 8 and the prior art, such advantages including

prolonging the useful life of the memory, increasing the pool of available physical blocks, and slowing the spreading of growing defects, also support the patentability of these claims over the Wells reference and the other art of record.

Applicants therefore submit that amended claim 8 and its dependent claims are novel and patentably distinct over the prior art of record.

Claim 13 is similarly amended as discussed above relative to claim 8, by now reciting that a memory system including, *inter alia,* code devices that identify a first logical block of a plurality of logical blocks, each including a plurality of logical pages arranged in groups, with the first logical block having contents associated with a number of groups of logical pages fewer than a first limit. No new matter is presented by this amendment, given the clear support in the specification.[12]

Claims 14 through 16 are amended for clarity, and for consistency with the amendment to claim 13, upon which they depend.

For similar reasons as discussed above relative to amended claims 1 and 8, Applicants submit that amended claim 13 and its dependent claims are novel and patentably distinct over the Wells reference and the other prior art of record in this case.

The novelty of amended claim 13 is evident because the Wells reference nowhere discloses any arrangement of a logical block in its flash memory, much less a logical block having logical pages arranged in groups, nor does it disclose any code devices that identify a first logical block by its contents being associated with a number of groups of logical pages fewer than a first limit, both as required by amended claim 13. Indeed, the Wells reference discloses no arrangement of logical blocks beyond its blocks that have odd and even data bytes stored in subblocks of different integrated circuits. The Wells reference therefore necessarily fails to disclose a logical block that includes a plurality of logical pages arranged in groups, as claimed. Given this lack of disclosure of the arrangement of logical blocks, the Wells reference

[12] *See,* specification, *supra, e.g.,* at page 11, lines 9 through 15.

necessarily fails to disclose code devices that can identify a first logical block by virtue of the number of its groups of logical pages associated with data being below a first limit. Accordingly, Applicants submit that the Wells reference falls short of the requirements of amended claim 13, and that therefore claims 13 through 19 are novel over the reference.

Applicants further submit that amended claim 13 and its dependent claims are not only novel, but are patentably distinct over the prior art because there is no suggestion to modify the teachings of the Wells reference in such a manner as to reach the claim. This lack of suggestion is evident from the substantial shortfall of the reference relative to the claimed memory system, and also because of the purely sequential approach to storing sectors of data followed by the Wells reference. Nor do the other references of record provide any suggestion in this regard. And considering that the important advantages provided by the invention of amended claim 13 are due to the differences between the claim and this prior art, Applicants submit that the memory system of amended claim 13 is substantially different from the art, and thus patentably distinct over this prior art.

Applicants therefore submit that amended claim 13 and its dependent claims 14 through 19 are both novel and patentably distinct over the prior art of record.

The prior art cited as pertinent but not applied has been considered, but is not felt to come within the scope of the claims in this case.

Applicants bring the references listed on the enclosed PTO/SB/08 to the attention of the Patent and Trademark Office relative to this application. These references were only recently cited in the PCT International Search Report of an application related to this application. A copy of that Search Report is also enclosed.

Copies of those references that are not U.S. Patents are enclosed.[13] The references are all in the English language. As such, no additional statement of relevance is provided in this paper.

[13] 37 C.F.R. §1.98(a)(2)(ii).

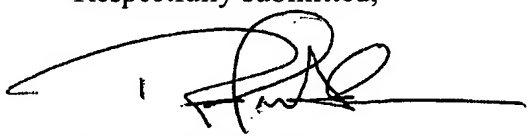
The fee for this Information Disclosure Statement is enclosed, as indicated in the Fee Transmittal filed with this paper.[14]

By citing these references, Applicants do not admit that any of these references is, or is considered to be, material to the patentability of any of the claims of this application.[15]

Consideration of this information in the examination of this application is respectfully requested.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



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[14] 37 C.F.R. §1.97(c)(2).
[15] 37 C.F.R. §1.97(h).